

REMARKS

Claims 1 to 20 are currently pending in the present application with claims 1 to 14 having been amended herein. The amendments to the claims do not present new matter.

Claims 1, 5 and 14 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,396,137 to Klughart (hereinafter "Klughart"). It is respectfully submitted that Klughart does not anticipate the subject matter of claims 1, 5 and 14 for the following reasons.

As regards the anticipation rejections of the claims, to reject a claim under 35 U.S.C. § 102(b), the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. (*See Scripps Clinic & Research Foundation v. Genentech, Inc.*, 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991))(emphasis added).

Claim 1 recites an interposer layer including voltage regulator elements, the interposer layer having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked **surface-to-surface** with the exposed surface layer. Klughart does not disclose this feature, but rather, plainly refers only to a system in which an insulating layer (1705) *separates* a voltage regulator/switch and a foundation integrated circuit. Klughart, col. 24, lines 60-62. In other words, in Klughart, since an insulating layer is positioned between the voltage regulator/switch and the foundation integrated circuit, the regulator is not stacked surface-to-surface with the exposed layer of the integrated circuit.

Moreover, the positioning of the insulating layer described in Klughart is not merely a matter of design choice since the silicon-on-insulator (SOI) fabrication technique used to produce the structure topology in Klughart **necessarily produces an insulating layer** in between the foundation integrated circuit and a conduction routing layer including a power supply. *See* Klughart, col. 27, line 62 to col. 28, line 11. Thus, Klughart not only does not disclose a surface-to-surface coupling between a voltage regulator and an integrated circuit but actually plainly teaches away from this structure.

For at least these reasons, Klughart does not anticipate the subject matter of independent claim 1.

As claims 5 and 14 recite features analogous to those of claim 1, it is submitted that Klughart also does not anticipate the subject matter of these claims.

Withdrawal of the anticipation rejection of claims 1, 5 and 14 is accordingly respectfully requested.

Claims 2-4, 6-9, and 15-20 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Klughart in view of U.S. Patent No. 6,137,164 to Yew et al. (hereinafter “Yew”). It is respectfully submitted that the combination of Klughart and Yew does not render obvious the subject matter of claims 2-4, 6-9 and 15-20.

Establishment of *prima facie* obviousness requires satisfaction of three separate criteria. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Each of claims 2-4, 6-9 and 15-20 depend from independent claims 1, 5 and 14 respectively. It is submitted that the Yew reference fails to cure the deficiencies of the primary Klughart reference in that it also does not disclose or suggest an interposer layer including voltage regulator elements having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked surface-to-surface with the exposed surface layer. In contrast, Yew merely discloses a rigid interposer printed circuit board that includes traces for interconnecting electrical terminals and does not include voltage regulator elements. See Yew, col. 4, lines 61-65.

As the combination of Klughart and Yew fails to disclose each of the elements of independent claims 1, 5 and 14, *a fortiori*, the combination of references relied upon fails to render obvious the subject matter of their dependent claims 2-4, 6-9 and 15-20.

Withdrawal of the obviousness rejection of claims 2-4, 6-9 and 15-20 is accordingly respectfully requested.

Claims 10-13 have been rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,262,905 to Zhang et al. (hereinafter “Zhang”) in view of U.S. Patent No. 6,265,771 to Ference et al. (hereinafter “Ference”). It is respectfully submitted that the combination of Zhang and Ference does not render obvious the subject matter of claims 10-13.

Claim 10 recites an interposer situated between the substrate and the integrated circuit die, the interposer having voltage regulator elements for receiving voltage from the power supply and for down-converting the voltage from the power supply into a regulated voltage. The Office Action relies on Ference as disclosing such an interposer structure. Respectfully, it is unclear what sections of the Ference reference that the Office Action bases its reliance on. Ference merely refers to integrating a heat sink into an integrated circuit, and does not mention or refer to an interposer between a substrate and an integrated circuit, let alone an interposer layer including voltage regulator elements as claimed. It is therefore submitted that the combination of Zhang and Ference fails to disclose or suggest each of the elements of independent claim 10 or its dependent claims 11-13.

Withdrawal of the obviousness rejection of claims 10-13 is accordingly respectfully requested.

CONCLUSION

All issues having been addressed, it is believed that the present application is in condition for allowance. Prompt reconsideration and allowance of the present application are respectfully requested.

Respectfully submitted,

KENYON & KENYON

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By: Howard I. Grossman
Howard I. Grossman
(Reg. No. 48,673)

KENYON & KENYON
One Broadway
New York, NY 10004
(212) 425-7200

CUSTOMER NO: 26646